VLSI IEEE PAPERS-2018

S.NO	CODE	TITLES	YEAR
1	CTVL01	Systematic Design of an Approximate Adder: The Optimized Lower Part Constant-OR Adder	2018
2	CTVL02	A Simple Yet Efficient Accuracy-Configurable Adder Design	2018
3	CTVL03	Low-Complexity VLSI Design of Large Integer Multipliers for Fully Homomorphic Encryption	2018
4	CTVL04	Approximate Hybrid High Radix Encoding for Energy-Efficient Inexact Multipliers	2018
5	CTVL05	An Efficient Fault-Tolerance Design for Integer Parallel Matrix–Vector Multiplications	2018
6	CTVL06	Sense-Amplifier-Based Flip-Flop With Transition Completion Detection for Low-Voltage Operation	2018
7	CTVL07	A Reconfigurable Cache for Efficient Use of Tag RAM as Scratch-Pad Memory	2018
8	CTVL08	FIR Filter Realization via Deferred End-Around Carry Modular Addition	2018
9	CTVL09	Modular Design of High-Efficiency Hardware Median Filter Architecture	2018
10	CTVL10	An Energy-Efficient Network-on-Chip-Based Reconfigurable Viterbi Decoder Architecture	2018
11	CTVL11	Towards a Dependable True Random Number Generator With Self-Repair Capabilities	2018
12	CTVL12	A Computationally Efficient Reconfigurable Constant Multiplication Architecture Based on CSD Decoded Vertical–Horizontal Common Sub-Expression Elimination Algorithm	2018
13	CTVL13	LFSR-Based Test Generation for Path Delay Faults	2018

14	CTVL14	On-Chip Self-Test Methodology with All Deterministic Compressed Test Patterns Recorded in Scan Chains	2018
15	CTVL15	DR-scan: Dual-rail Asynchronous Scan DfT and ATPG	2018
16	CTVL16	On-Chip Diagnosis of Generalized Delay Failures using Compact Fault Dictionaries	2018
17	CTVL17	Double MAC on a DSP: Boosting the Performance of Convolutional Neural Networks on FPGAs	2018
18	CTVL18	Secure Double Rate Registers as an RTL Countermeasure Against Power Analysis Attacks	2018
19	CTVL19	Low Overhead Warning Flip-Flop Based on Charge Sharing for Timing Slack Monitoring	2018
20	CTVL20	An Adaptive Mechanism for Designing Efficient Snoop Filters	2018
21	CTVL21	Toward Energy-Efficient Stochastic Circuits Using Parallel Sobol Sequences	2018
22	CTVL22	On the Analysis and the Mitigation of Power Supply Noise and Power Distribution Network Impedance Variation for Scan-Based Delay Testing Techniques	2018
23	CTVL23	Design of Area-Efficient and Highly Reliable RHBD 10T Memory Cell for Aerospace Applications	2018
24	CTVL24	A Flexible and Energy-Efficient Convolutional Neural Network Acceleration With Dedicated ISA and Accelerator	2018
25	CTVL25	Low-Cost Lifting Architecture and Lossless Implementation of Daubechies-8 Wavelets	2018
26	CTVL26	A Method to Detect Bit Flips in a Soft-Error Resilient TCAM	2018
27	CTVL27	Fault Group Pattern Matching with Efficient Early Termination for High-Speed Redundancy Analysis	2018

28	CTVL28	Bitstream Fault Injections (BiFI) – Automated Fault Attacks against SRAM-based FPGAs	2018
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33	CTVL33	Improving Error Correction Codes for Multiple-Cell Upsets in Space Applications	2018