VLSI IEEE PAPERS-2017

S.NO	CODE	TITLES	YEAR
1	CTVL01	Content Addressable Memory—Early Predict and Terminate Precharge of Match-Line	2017
2	CTVL02	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing	2017
3	CTVL03	Design of Efficient BCD Adders in Quantum Dot Cellular Automata	2017
4	CTVL04	Efficient Designs of Multiported Memory on FPGA	2017
5	CTVL05	Power-Gated 9T SRAM Cell for Low-Energy Operation	2017
6	CTVL06	Efficient Designs of Multiported Memory on FPGA	2017
7	CTVL07	Register Less Null Conversion Logic	2017
8	CTVL08	Energy-Efficient TCAM Search Engine Design Using Priority-Decision in Memory Technology	2017
9	CTVL09	Energy-Efficient Adaptive Match-Line Controller for Large-Scale Associative Storage	2017
10	CTVL10	A Hybrid Time Borrowing Technique to Improve the Performance of Digital Circuits in the Presence of Variations	2017
11	CTVL11	An Efficient Component for Designing Signed Reverse Converters for a Class of RNS Moduli Sets of Composite Form $\{2k, 2P-1\}$	2017
12	CTVL12	Design of Power and Area Efficient Approximate Multipliers	2017
13	CTVL13	Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers	2017
14	CTVL14	Reliable Low-Latency Viterbi Algorithm Architectures Benchmarked on ASIC and FPGA	2017
15	CTVL15	Test Stimulus Compression Based on Broadcast Scan with	2017

		One Single Input	
16	CTVL16	Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication	2017
17	CTVL17	Optimized Design of an LSSD Scan Cell	2017
18	CTVL18	Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test Pattern Generation and Reseeding	2017
19	CTVL19	A Memory-Based FFT Processor Design With Generalized Efficient Conflict-Free Address Schemes	2017
20	CTVL20	An Improved DCM-based Tunable True Random Number Generator for Xilinx FPGA	2017
21	CTVL21	Seven-bit 700-MS/s Four-Way Time-Interleaved SAR ADC With Partial *V*cm-Based Switching	2017
22	CTVL22	High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations	2017
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24	CTVL24	Low Latency and Low Error Floating-Point Sine/Cosine Function Based TCORDIC Algorithm	2017
25	CTVL25	Hardware/Software Approach to Designing Low-Power RNS-Enhanced Arithmetic Units	2017
26	CTVL26	Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test Pattern Generation and Reseeding	2017
27	CTVL27	Novel Radiation-Hardened-by-Design (RHBD) 12T Memory Cell for Aerospace Applications in Nanoscale CMOS Technology	2017
28	CTVL28	Overloaded CDMA Crossbar for Network-On-Chip	2017
29	CTVL29	Resource-Efficient SRAM-based Ternary Content Addressable Memory	2017

30	CTVL30	Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST	2017
31	CTVL31	Selecting Replacements for Undetectable Path Delay Faults	2017
32	CTVL32	Test Stimulus Compression Based on Broadcast Scan with One Single Input	2017
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36	CTVL36	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	2016
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