NO	TITLE	YEAR
CLVLSI-01	An Accuracy-Adjustment Fixed-Width Booth Multiplier Based on Multilevel Conditional Probability	JAN 2015
CLVLSI-02	Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications	JAN 2015
CLVLSI-03	Recursive Approach to the Design of a Parallel Self-Timed Adder	JAN 2015
CLVLSI-04	Razor Based Programmable Truncated Multiply and Accumulate, Energy-Reduction for Efficient Digital Signal Processing	JAN 2015
CLVLSI-05	Reliable Low-Power Multiplier Design Using Fixed-Width Replica Redundancy Block	JAN 2015
CLVLSI-06	Aging Adaption in Integrated Circuits Using a Novel Built-In Sensor	JAN 2015
CLVLSI-07	Novel Design Algorithm for Low Complexity Programmable FIR Filters Based on Extended Double Base Number System	JAN 2015
CLVLSI-08	Security Vulnerabilities of Emerging Nonvolatile Main Memories and Countermeasures	JAN 2015
CLVLSI-09	Exploiting Same Tag Bits to Improve the Reliability of the Cache Memories	FEB 2015
CLVLSI-10	Fault Tolerant Parallel Filters Based on Error Correction Codes	FEB 2015
CLVLSI-11	Reverse Converter Design via Parallel-Prefix Adders: Novel Components, Methodology, and Implementations	FEB 2015
CLVLSI-12	Z-TCAM: An SRAM-based Architecture for TCAM	FEB 2015
CLVLSI-13	Design of an Ultra-low Voltage 9T SRAM With Equalized Bitline Leakage and CAM-Assisted Energy Efficiency Improvement	FEB 2015
CLVLSI-14	A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable Orthogonal Approximation of DCT	FEB 2015
CLVLSI-15	Aggressive Voltage Scaling Through Fast Correction of Multiple Errors With Seamless Pipeline Operation	FEB 2015
CLVLSI-16	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic	MAR 2015
CLVLSI-17	Designing a SAR-Based All-Digital Delay-Locked Loop With Constant Acquisition Cycles Using a Resettable Delay Line	MAR 2015
CLVLSI-18	Diagnosis and Layout Aware (DLA) Scan Chain Stitching	MAR 2015
CLVLSI-19	A 3.6-mW 50-MHz PN Code Acquisition Filter via Statistical Error Compensation in 180-nm CMOS	MAR 2015
CLVLSI-20	Skewed-Load Test Cubes Based on Functional Broadside Tests for a Low-Power Test Set	MAR 2015

NO	TITLE	YEAR
CLVLSI-21	Fine-Grained Critical Path Analysis and Optimization for Area-Time Efficient Realization of Multiple Constant Multiplications	MAR 2015
CLVLSI-22	An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis	APR 2015
CLVLSI-23	Low-Power Clock Distribution Using a Current-Pulsed Clocked Flip-Flop	APR 2015
CLVLSI-24	Array-Based Approximate Arithmetic Computing: A General Model and Applications to Multiplier and Squarer Design	APR 2015
CLVLSI-25	Asynchronous Domino Logic Pipeline Design Based on Constructed Critical Data Path	APR 2015
CLVLSI-26	Algorithm and Architecture for a Low-Power Content-Addressable Memory Based on Sparse Clustered Networks	APR 2015
CLVLSI-27	Randomized Multitopology Logic Against Differential Power Analysis	APR 2015
CLVLSI-28	A Low-Latency and Low-Power Hybrid Scheme for On-Chip Networks	APR 2015
CLVLSI-29	A Low-Cost Low-Power All-Digital Spread-Spectrum Clock Generator	MAY 2015
CLVLSI-30	Fine-Grained Fast Field-Programmable Gate Array Scrubbing	MAY 2015
CLVLSI-31	Design of Efficient Content Addressable Memories in High-Performance FinFET Technology	MAY 2015
CLVLSI-32	A 0.325 V, 600-kHz, 40-nm 72-kb 9T Subthreshold SRAM with Aligned Boosted Write Wordline and Negative Write Bitline Write-Assist	MAY 2015
CLVLSI-33	A Combined SDC-SDF Architecture for Normal I/O Pipelined Radix-2 FFT	MAY 2015
CLVLSI-34	A Class of SEC-DED-DAEC Codes Derived From Orthogonal Latin Square Codes	MAY 2015
CLVLSI-35	Variable Latency Speculative Han-Carlson Adder	MAY 2015
CLVLSI-36	Low-Power and Area-Efficient Shift Register Using Pulsed Latches	JUNE 2015
CLVLSI-37	Energy-Efficient Approximate Multiplication for Digital Signal Processing and Classification Applications	JUNE 2015
CLVLSI-38	A High-Performance On-Chip Bus (MSBUS) Design and Verification	JULY 2015
CLVLSI-39	Scan Chain Masking for Diagnosis of Multiple Chain Failures in a Space Compaction Environment	JULY 2015
CLVLSI-40	VLSI Design for SVM-Based Speaker Verification System	JULY 2015

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CLVLSI-41	Code Compression for Embedded Systems Using Separated Dictionaries	FP 2015
CLVLSI-42	Design for Testability of Sleep Convention Logic	FP 2015
CLVLSI-43	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	FP 2015
CLVLSI-44	WCET-Aware Energy-Efficient Data Allocation on Scratchpad Memory for Real-Time Embedded Systems	FP 2015
CLVLSI-45	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic	FP 2015
CLVLSI-46	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	FP 2015
CLVLSI-47	An FPGA Architecture and CAD Flow Supporting Dynamically Controlled Power Gating	FP 2015
CLVLSI-48	Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication	FP 2015
CLVLSI-49	Low-Cost Multiple Bit Upset Correction in SRAM-Based FPGA Configuration Frames	FP 2015
CLVLSI-50	A Performance Degradation Tolerable Cache Design by Exploiting Memory Hierarchies	FP 2015
CLVLSI-51	In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers	FP 2015
CLVLSI-52	A Novel Quantum-Dot Cellular Automata X-bit ×32-bit SRAM	FP 2015
CLVLSI-53	Reliable and Error Detection Architectures of Pomaranch for False-Alarm-Sensitive Cryptographic Applications	FP 2015
CLVLSI-54	A High-Speed FPGA Implementation of an RSD-Based ECC Processor	FP 2015
CLVLSI-55	Scalable Elliptic Curve Cryptosystem FPGA Processor for NIST Prime Curves	FP 2015
CLVLSI-56	A Single-Ended With Dynamic Feedback Control 8T Subthreshold SRAM Cell	FP 2015
CLVLSI-57	VLSI-Assisted Nonrigid Registration Using Modified Demons Algorithm	FP 2015