NO	TITLE	YEAR
CLVLSI-01	A Mixed-Decimation MDF Architecture for Radix-2*k* Parallel FFT	JAN 2016
CLVLSI-02	An FPGA Architecture and CAD Flow Supporting Dynamically Controlled Power Gating	JAN 2016
CLVLSI-03	Code Compression for Embedded Systems Using Separated Dictionaries	JAN 2016
CLVLSI-04	In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers	JAN 2016
CLVLSI-05	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	FEB 2016
CLVLSI-06	A Method to Design Single Error Correction Codes With Fast Decoding for a Subset of Critical Bits	FEB 2016
CLVLSI-07	A Performance Degradation Tolerable Cache Design by Exploiting Memory Hierarchies	FEB 2016
CLVLSI-08	Design for Testability of Sleep Convention Logic	FEB 2016
CLVLSI-09	Efficient Dynamic Virtual Channel Organization and Architecture for NoC Systems	FEB 2016
CLVLSI-10	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	FEB 2016
CLVLSI-11	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	FEB 2016
CLVLSI-12	Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication	FEB 2016
CLVLSI-13	High-Speed Hardware Implementation of Fixed and Runtime Variable Window Length 1-D Median Filters	MAR 2016

CLVLSI-14	An FPGA Implementation for Solving the Large Single-Source-Shortest-Path Problem	MAR 2016
CLVLSI-15	High-Performance Deadlock-Free ID Assignment for Advanced Interconnect Protocols	MAR 2016
CLVLSI-16	Low-Cost Multiple Bit Upset Correction in SRAM-Based FPGA Configuration Frames	MAR 2016
CLVLSI-17	Functional Test Generation for Hard-to-Reach States Using Path Constraint Solving	JUN 2016
CLVLSI-18	Low-Cost Low-Power Ring Oscillator-Based Truly Random Number Generator for Encryption on Smart Cards	JUN 2016
CLVLSI-19	EMDBAM: A Low-Power Dual Bit Associative Memory With Match Error and Mask Control	FUT
CLVLSI-20	LUT Optimization for Distributed Arithmetic-Based Block Least Mean Square Adaptive Filter	FUT